# Design of a Ring-Type SC DC-DC Converter for Diode-Lamps in Cellular Phones 

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#### Abstract

A ring-type switched-capacitor (SC) DC-DC converter for diode-lamps in cellular phones is proposed in this paper. To achieve high efficiency, the bootstrap circuits are attached to power-switches in the converter. By connecting the charged-capacitor between the gate terminal and the source terminal of the power-switch, the bootstrap circuit reduces the onresistance of the power-switch. Furthermore, the output voltage of the circuit is regulated by controlling the frequency of the clock pulse. To achieve high accuracy of the voltage control, the regulator is designed by a digital technique. Concerning a 3 -stage power converter, SPICE simulations are performed to confirm the validity of the circuit design. For the input voltage $3.2 \sim 4.5 \mathrm{~V}$, the power efficiency of the proposed circuit is $68 \sim 85 \%$ in the output current about 150 mA .


## 1. Introduction

A power converter is one of the most important building blocks in electronic products. In the design of the converters, most of them exploit magnetic elements. Although these converters can achieve high efficiency, the magnetic elements cause the increase of volume and weight. For this reason, switchedcapacitor (SC) power converters have been receiving much attentions in the field of mobile equipments, because the equipments such as cellular phone, digital camera, etc. require thin circuit composition, lightweight and low-noise. The SC power converters can satisfy these requirements since they consist of only capacitors and power switches [1]-[3]. In the SC power converters, the design of a power switch is important. To achieve high efficiency and small number of powerswitches, the gate terminals of power-switches must be driven by higher voltages than that of the source terminals. For this reason, we employ the power switches with bootstrap circuits to reduce the on-resistance of power-switches.


Fig. 1 Ring-type power converter.

In this paper, a ring-type switched-capacitor (SC) DC-DC converter for diode-lamps in cellular phones is proposed. Since the output voltage of the SC power converters is determined by the number of capacitors, the output voltage of the power converter is regulated by controlling the frequency of the clock pulse. In the design of the diode-lamps, $3 \%$ of realization accuracy is required for the output voltage of the power converter. Therefore, to achieve high accuracy of the voltage control, the regulator is designed by using a digital technique. Furthermore, to achieve high efficiency, the bootstrap circuits are attached to power-switches in the converter. By connecting the charged-capacitor between the gate terminal and the source terminal of the power-switch, the bootstrap circuit reduces the onresistance of the power-switch. Concerning a 3 -stage power converter, SPICE simulations are performed to confirm the validity of the circuit design.


Fig. 2 3-stage ring-type converter.

## 2. Circuit Structure

### 2.1. Ring-type DC-DC Converter

Figure 1 shows the ring-type power converter proposed by Hara et al.[1]. By controlling the powerswitches $S_{i, j}((i=1, \ldots, 4)$ and $(j=1,2, \ldots, N))$, the circuit converts a voltage to other by means of changing the connections of capacitors $C_{j}$ 's. The clock pulses for $S_{i, j}$ are non-overlapped $N$-phase pulses $\Phi_{i, j}$, and the clock pulses for $S_{2, j}$ are set to the inverted pulses of $\Phi_{1, j}$. The switches $S_{3, j}$ and $S_{4, j}$ are driven by the clock pulses obtained by shifting the clock-pulses $\Phi_{1, j}$ cyclically. When the output current is 0 and the voltage-drop caused by power-switches is free, the output voltage $V_{\text {out }}(t)$ is given by

$$
\begin{equation*}
V_{\text {out }}(t)=\frac{Q}{P} V_{\text {in }}, \tag{1}
\end{equation*}
$$

where $P \in\{1,2, \ldots, N\}$ and $Q \in\{1,2, \ldots, N\}$. In Eq.(1), $P$ and $Q$ denote the number of the capacitors connected to the input terminal and the output terminal, respectively. The parameters $P$ and $Q$ are determined by the timing of the clock pulses for $S_{3, j}$ and $S_{4, j}$, respectively.

As Eq.(1) shows, the ring-type power converter works as a step-up/step-down DC-DC converter by controlling the ratio of $P$ and $Q$. However, to realize step-up/step-down conversion, the gate terminals of $S_{2, j}, S_{3, j}$ and $S_{4, j}$ must be driven by higher voltages than that of the source terminals. Because a threshold voltage drop is occurred by the power switches. To avoid the threshold voltage drop, bootstrap circuits are employed in the proposed converter.


Fig. 3 Bootstrap circuit. (a) Bootstrap circuit-1. (b) Bootstrap circuit-2.

### 2.2. Proposed Converter

Figure 2 shows the proposed ring-type converter when $N=3$. In the circuit, the bootstrap circuits shown in Fig. 3 are attached to power-switches in the converter. The circuit shown in Fig. 3 (a) works as follows. During $\Phi_{\text {in }}$ is Low, the MOS-switches M1, M4, M5 and M7 are On, and M2, M3 and M6 are Off. In this timing, the capacitor $C_{b}$ is charged by $V_{i n}$. On the other hand, during $\Phi_{\text {in }}$ is High, the states of MOSswitches M1~M7 are reversed. Via M3 and M6, the gate terminal of the power switch is driven by the output voltage $V_{\text {clk }}$. When the voltage-drops caused by MOS-switches are $0, V_{c l k}$ is given by

$$
V_{c l k}=\left\{\begin{array}{ccc}
V_{i n}+V_{a} & \text { if } & \Phi_{\text {in }}=\text { High },  \tag{2}\\
0 & \text { if } & \Phi_{\mathrm{in}}=\text { Low } .
\end{array}\right.
$$

Thus, the gate terminals of power-switches are driven by higher voltages than that of the source terminals. The threshold voltage drop can be alleviated by the proposed bootstrap circuit.

To alleviate the threshold voltage drop, several techniques have been proposed in the previous studies $[2],[3]$. Among others, the output pulse of the conventional bootstrap circuit in [2] can also be expressed as shown in Eq.(2). The conventional circuit in [2] consists of 11 MOSFET's and 3 capacitors. As Fig.3(a) shows, the proposed bootstrap circuit is constructed with only 5 MOSFET's and a capacitor. Therefore,


Fig. 4 PWM controller.
the proposed bootstrap circuit can reduce the hardware cost.

The bootstrap circuit- 2 works as in the same manner of bootstrap circuit-1. In this circuit, $V_{\text {con }}(t)$ denotes the PWM signal which is given by PWM controller shown in Fig.4. By controlling $V_{\text {con }}(t)$, the output voltage $V_{\text {out }}(t)$ is regulated. When the output current is 0 and the voltage-drop caused by power-switches is free, the output voltage $V_{\text {out }}(t)$ of the proposed converter is given by

$$
\begin{equation*}
V_{\text {out }}(t)=\alpha\left(\frac{Q}{P}\right) V_{\text {in }} \tag{3}
\end{equation*}
$$

where $\alpha(\in[0,1])$ is a dumping factor which is determined by $V_{\text {con }}(t)$. The operations of the PWM controller will be described in the following subsection.

### 2.3. PWM Controller

To achieve high accuracy of the voltage control, the PWM controller of Fig. 4 is designed by a digital technique ${ }^{1}$. In Fig.4, the output voltage $V_{\text {out }}(t)$ is compared with the reference voltages $V_{z h}$ and $V_{z l}$ which are provided by Zener diodes, where $V_{z h}$ and $V_{z l}$ are an upper-limit and a lower-limit of the desired output voltage, respectively. When $V_{z h}<V_{\text {out }}(t)$, the $M$ bits register-1 is shifted 1-bit to the right by the signal RSC, and $1\left(=V_{\text {in }}\right)$ is inputted from RSI. On the other hand, when $V_{z l}>V_{\text {out }}(t)$, the register is shifted 1-bit to the right by the signal LSC, and $0(=0 \mathrm{~V})$ is inputted from LSI. The clock pulse to shift the register-1 is generated by $K$-bits counter $(K=1,2, \ldots)$. When $V_{z l} \leq V_{\text {out }}(t) \leq V_{z h}$, the clock pulses for the registers

[^0]

Fig. 5 Transient characteristic of bootstrap circuits. (a) Bootstrap circuit-1. (b) Bootstrap circuit-2.
are stopped. By using the outputs of register-1, $r_{k}$ $(k=1,2, \ldots, M)$, the PWM signal $V_{\text {con }}(t)$ is given by

$$
\begin{equation*}
V_{c o n}(t)=\overline{\left(c_{1} \cap r_{1}\right) \cup\left(c_{2} \cap r_{2}\right) \cup \cdots \cup\left(c_{M} \cap r_{M}\right)}, \tag{4}
\end{equation*}
$$

where $c_{k}$ is a non-overlapped $M$-phase pulse (see in Fig.4). The frequency of $c_{k}$ is set to $N \times M \times R$ times frequency of $\Phi_{1,1}$. As Eq. (4) shows, the duty factor of $V_{\text {con }}(t)$ is changed according to the states of $r_{k}$ 's. The parameter $\alpha$ in Eq.(3) is proportioned to the duty factor of $V_{\text {con }}(t)$.

## 3. Simulation

To confirm the validity of the circuit design, SPICE simulations were performed concerning the circuits shown in Fig.2. The SPICE simulations were performed under the conditions that the input voltage $V_{i n}=3.2 \sim 4.5 \mathrm{~V}, V_{z h}=5.0 \mathrm{~V}, V_{z l}=4.5 \mathrm{~V}^{2}$, $C_{j}=C_{o}=5 \mu F, C_{b}=2 n F, R_{o}=30 \Omega$, the parameter $M=8, R=2, K=2$, and the on-resistance of the power-switch $R_{o n}=1.8 \Omega$.

Figure 5 shows the transient characteristics of the bootstrap circuits. In Fig. 5 (b), the duty factor of $V_{\text {con }}(t)$ was set to 0.2 . As these figures show, the pulse width of the output of the bootstrap circuit-2 is modulated. Figure 6 shows the transient characteristics of the proposed converter. In these simulations, the clock pulses for the power switches were set to satisfy

[^1]

Fig. 6 Transient characteristic of the proposed power converter. (a) $V_{i n}=3.6 \mathrm{~V}$. (b) $V_{i n}=3.2 \mathrm{~V}$. (c) $V_{i n}=$ 4.5 V .
the following conditions that $\Phi_{1,1}=\overline{\Phi_{2,1}}=\Phi_{3,2}=$ $\Phi_{4,3}, \Phi_{1,2}=\overline{\Phi_{2,2}}=\Phi_{3,3}=\Phi_{4,1}$, and $\Phi_{1,3}=\overline{\Phi_{2,3}}=$ $\Phi_{3,1}=\Phi_{4,2}$. In other word, the parameters $P$ and $Q$ in Eq.(3) were set to 2 and 3, respectively. As Fig. 6 shows, the settling time of the converter is less than $500 \mu \mathrm{~s}$. Figures 7 and 8 show the efficiency and the output voltage of the power converter, respectively. As Figs. 7 and 8 show, the proposed converter can provide the output voltage in the range of $4.5 \sim 5.0 \mathrm{~V}$. Of course, the accuracy of the output voltage $V_{\text {out }}(t)$ can be improved by increasing the bit-length of the register-1. The power efficiency is $68 \sim 85 \%^{3}$ in the output current about 150 mA .

[^2]

Fig. 7 Power efficiency.


Fig. 8 Output voltage $V_{\text {out }}(t)$.

## 4. Conclusion

A ring-type switched-capacitor (SC) DC-DC converter for diode-lamps in cellular phones has been proposed in this paper.

The SPICE simulations showed the following results. 1. For the input voltage $3.2 \sim 4.5 V$, the power efficiency of the proposed circuit is $68 \sim 85 \%$ in the output current about 150 mA . 2. The material cost for the bootstrap circuit is smaller than that for the conventional circuit. 3. The converter can achieve high accuracy of the voltage control since the voltage controller is designed by a digital technique.

The further improvement of efficiency is left to the future study.

## References

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[3] K.Eguchi, H.Zhu, T.Tabata and F.Ueno, "A Dickson-type power converter with bootstrapped gate transfer switches," Proc. of the 25th International Telecommunications Energy Conference, pp.623-626, Oct. 2003.


[^0]:    ${ }^{1}$ In the design of the diode-lamps, $3 \%$ of realization accuracy is required for the output voltage of the power converter.

[^1]:    ${ }^{2}$ We focused on the diode-lamp whose dynamic range is $4.5 \sim$ 5 V . The typical input and output voltages are 3.6 V and 4.75 V , respectively.

[^2]:    ${ }^{3}$ The power efficiency of the proposed converter can be improved by using the power-switches with small on-resistance. Under the same range of the input and the output voltages, the power efficiency of the conventional converters for diode lamps is about $65 \%$.

