A TDM Cyclic Sigma Delta ADC

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Abstract— It was proposed previously cyclic type of sigma delta ADC that a feedback line is equipped with a conventional sigma delta ADC for improving resolution and reducing conversion time. And also TDM (Time Division Multiplexing) cyclic sigma delta ADC architecture was proposed mathematically on previous research. In this paper, TDM Cyclic Sigma Delta ADC is realized by major circuit simulator.

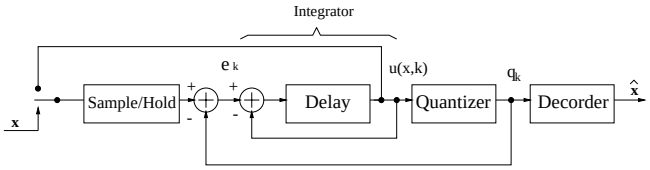

Figure 1: Block Diagram of Cyclic Sigma Delta ADC.

1. Introduction

As the chip integration advances toward the VLSI/ ULSI integrated systems, on-chip analog-digital interfaces are essential. One of the key technologies in analog-digital interfaces design is the low cost and high performance analog-digital data conversion, especially the high resolution analog-to-digital (A/D) conversion. High resolution A/D converters are required in many applications, such as scientific and medical instruments, process control, digital audio, and so on. To realize them, the switched-capacitor (SC) technique has been widely used because the matching accuracy of capacitors is superior to that of resistors. The highly precise conversion technique for the signal of a voice band, sigma delta ADC has been attracted attention instead of successive approximation ADC, that consists of simple circuit and has the excellent characteristics, which is robust parasitic effects and capacitor matching. By the above reasons, SC based Sigma delta ADC suits monolithic implementation. Recently, the study of sigma delta ADC tends to make Over Sampling Ratio higher and make complicate high order digital filters. Accelerating sigma delta ADC neither complicate construction nor much elements is demanded in commercial market. It was proposed novel cyclic type of sigma delta ADC[2] that a feedback line is equipped with a conventional sigma delta ADC[1] for improving the resolution and conversion time[3]. It is constructed by compact circuit, so it focuses the research in this time. Previous work realized circuit of circulated only one time, and proposed architecture of multiplexing more than 2 times mathematically. In this paper, achieved TDM cyclic sigma delta ADC with SC circuit and Unity Gain Buffer (UGB) that has been constructed by modifying circuit and modifying SC clock timing which introduce new technique of feedback residue voltage from integrator outputs. It is evaluated by Cadence Pspice A/D circuit simulator.

2. Cyclic Sigma Delta ADC

2.1. A Cyclic Digma Delta ADC

A Cyclic sigma delta ADC is shown in Figure.1, it consists of a sample hold, an analog integrator, with 1-bit quantizer and decoder. The analog feedback line is equipped with Conventional sigma delta ADC[1]. An analog input voltage x is limited by range of reference voltage as V_{REF},

$$-V_{REF} < x < +V_{REF} \tag{1}$$

assumes k-th sigma delta operations, input of integrator and output of integrator is expressed by e_k and $u(x,k)$ respectively, the differential equation as

$$e_k = x - q_k \tag{2}$$

$$u(x,k) - u(x,k-1) = e_{k-1} \tag{3}$$

with the initial condition, $u(x,0) = 0$. The quantizer output q_k is defined by

$$q_k = \begin{cases} +V_{REF} & u(x,k) \geq 0, \\ -V_{REF} & u(x,k) < 0. \end{cases} \tag{4}$$

Table 1: Performance of cyclic sigma delta ADC

(m, n)	Conventional	Cyclic	improved
(4, 8)	-18.1dB/3bit	-24.1dB/ 4bit	6.0dB
(8,16)	-24.1dB/4bit	-36.1dB/ 6bit	12.0dB
(16,32)	-30.1dB/5bit	-48.2dB/ 8bit	18.1dB
(32,64)	-36.1dB/6bit	-60.2dB/10bit	24.1dB
(64,128)	-42.1dB/7bit	-72.2dB/12bit	30.1dB
(128,256)	-48.2dB/8bit	-84.3dB/14bit	36.1dB
(256,512)	-54.1dB/9bit	-96.2dB/16bit	42.1dB

From (2),(3) and (4), the analog input x is converted to the digital value while conversion, equation is given by

$$x = \frac{1}{n}\sum_{k=0}^{n-1} q_k + \frac{1}{n}u(x,n) \tag{5}$$

The first component on the RHS of (5) gives the digital equivalent value will pass to decoder from quantizer, and the second component on the RHS of (5) gives the quantization error in the conversion. Theoretically, an analog input voltage is converted to $\log_2 n$ bit digital output during number of n operations, the quantization error is shown by

$$20 \cdot \log_{10}\left|\frac{u(x,n)}{n \cdot V_{REF}}\right| \quad [dB] \tag{6}$$

A cyclic sigma delta ADC defines number of n operations divide into 2 blocks as both m operations and l operations where $n = m + l$. The residue voltage of integrator output at the end of first block(m-th operation) transfers to sample hold as ADC input for the second block(l operations) via feedback line. The equation after first block is

$$x = \frac{1}{m}\sum_{k=0}^{m-1} q_k + \frac{1}{m}u(x,m) \tag{7}$$

Then, the second block equation is shown by

$$u(x,m) = \frac{1}{l}\sum_{k=m}^{n-1} q_k + \frac{1}{l}u(u(x,m),l) \tag{8}$$

Hence, cyclic method equation can be derived from (7) and (8) as

$$x = \frac{1}{m}\sum_{k=0}^{m-1} q_k + \frac{1}{m\cdot l}\left\{\sum_{k=m}^{n-1} q_k + u(u(x,m),l)\right\} \tag{9}$$

2 blocks cyclic scheme gets best performance when operation number sets $m = l = n/2$, the accuracy comparison is shown in Table.1 [3]

2.2. TDM Cyclic Sigma Delta ADC

Further cyclic multiplexing is able to realize when the residue voltage of integrator output goes back iterative more than 2 times as ADC input. It meant the last component on the RHS of (9) inputs to sample hold. In the case of the total operation number n divides into the d-th power of 2 blocks,

$$n = \sum_{i=1}^{d} m_i \tag{10}$$

the TDM cyclic method equation is generalized by[3]

$$x = \sum_{i=1}^{d}\sum_{m_{(i-1)}}^{m_i-1}\frac{q_k}{\prod_i} + \frac{u(u(\cdots, m_{d-1}-m_{d-2}), m_d - m_{d-1})}{\prod_d} \tag{11}$$

where $\prod_i = (m_i - m_{i-1}) \times \cdots \times (m_2 - m_1) \times m_1$

3. Inverse Integrator Output

Because of the residue voltage of integrator output $u(x,k)$ often beyond more than $|V_{REF}|$ during sigma delta operation, the TDM cyclic method has not been implemented yet. In this condition, $u(x,k)$ will be oscillation on the cyclic sigma delta ADC. In fact, $u(x,k)$ range should be

$$-2V_{REF} < u(x,k) < +2V_{REF} \tag{12}$$

The problem may occur while the input voltage is not equivalent to 0 and $u(x,k) = 0$ during the sigma delta operation. If it happens on the last operation of the block, input voltage of ADC does not match the input limitation as equation (1). On this regard, proposes new algorithm for the circuit implementation which is inverse integrator output. If the value of u(x,k) inverts polarity when it inputs the sample hold as next block sigma delta operation, TDM cyclic sigma delta ADC can act expecting the behavior properly. Both the inverted $u(x,k)$ and delayed feedback reference voltage offset each other, it does not exceed the $|V_{REF}|$. To invert $u(x,k)$, the equations have to be modified. It is solved by multiplying minus twice to quantization error term on the equations, so the equation (9) and the equation (11) are arranged as;

$$x = \frac{1}{m}\sum_{k=0}^{m-1} q_k - \frac{1}{m\cdot l}\left\{-\sum_{k=m}^{n-1} q_k - u(u(x,m),l)\right\} \tag{13}$$

$$\begin{aligned} x &= \sum_{i=1}^{d}(-1)^{i+1}\sum_{m_{(i-1)}}^{m_i-1}\frac{q_k}{\prod_i} \\ &- \frac{u(u(\cdots, m_{d-1}-m_{d-2}), m_d - m_{d-1})}{\prod_d} \end{aligned} \tag{14}$$

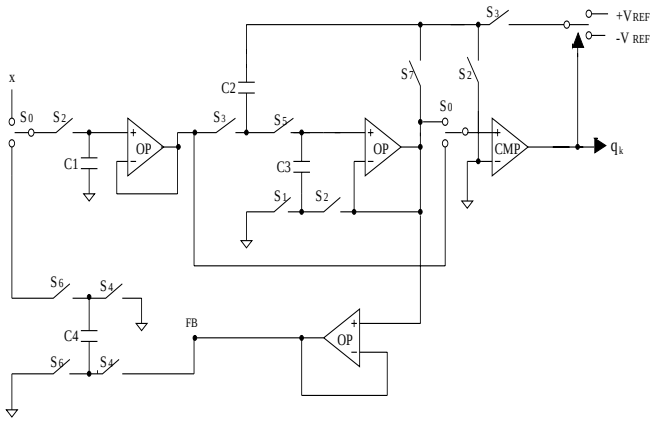

Figure 2: Circuit diagram of Cyclic sigma delta.

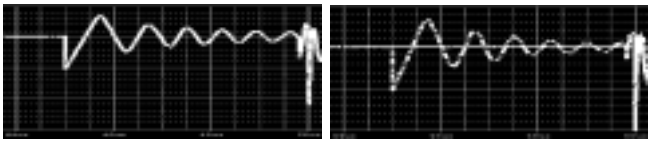

Figure 3: Improvement of Inverse Integrator Output. left: no buffer op-amp , right: with the buffer op-amp. Point FB voltage is broken line, Integrator output voltage is solid line.

4. TDM Cyclic Sigma Delta ADC Circuit

In this paper, it changed circuit design for realizing SC TDM cyclic sigma delta ADC more than two blocks. The circuit diagram is shown in Figure.2. The circuit is consisted to 3 op-amps, 1 comparator, 4 capacitors, 18 analog switches and 1 inverter. One op-amp is used by SC integrator, another one op-amp is for sample hold, and lest one op-amp is used for inverting the integrator output. On the Figure.2, analog signal is inputed from left upper side, switch S2, capacitor C1 and UGB op-amp is sample hold circuit where it closes to the analog input, capacitor C4, 2 S6 switches and 2 S4 switches locate left bottom side which is the inverse integrator output circuit, the center bottom UGB op-amp is the buffer between integrator and voltage inverting circuit, center middle UGB op-amp is integrator, the comparator is in right side, the reference voltage is inputed from right upper side. The clock timing chart of 2 blocks cyclic and 4 blocks cyclic is shown in Figure.4 and Figure.5, respectively. Both 2 blocks cyclic and 4 blocks cyclic need 9 kind of clock phases, both differences are S1, S2, S4, S6 and S7, all of them control to divide cyclic blocks. The UGB op-amp for inverse integrator output circuit keeps integrator output voltage steadily. If it does

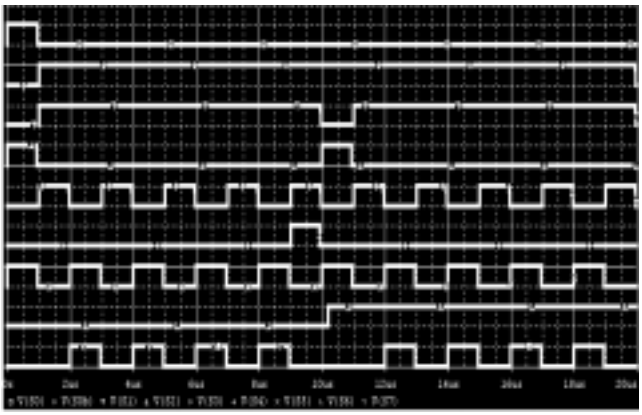

Figure 4: Clock timing chart of 2 blocks cyclic. Clock timings are $S0, \overline{S0}, S1, S2, S3, S4, S5, S6$ and $S7$ to the turn from a top.

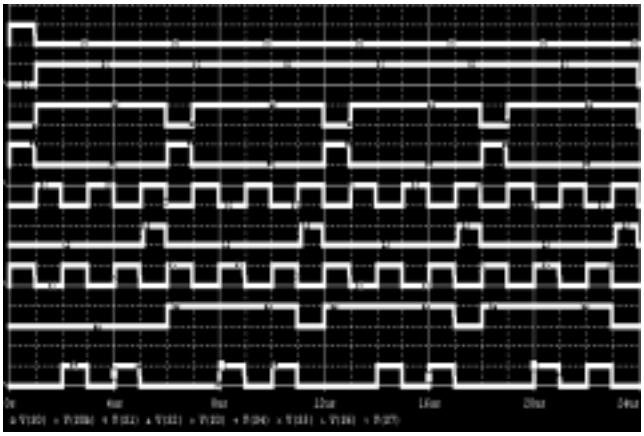

Figure 5: Clock timing chart of 4 blocks cyclic. Clock timings are $S0, \overline{S0}, S1, S2, S3, S4, S5, S6$ and $S7$ to the turn from a top.

not equip with the buffer op-amp on circuit, integrator output is swing. Figure.3 shows in the cases of both no buffer op-amp and with the buffer op-amp on circuit, both the point of FB and the voltage of integrator output are swinging on the without buffer op-amp condition, contrastively the voltage of integrator output keeps its voltage on with the buffer op-amp on circuit. Extra 1 op-amp is essential. Generally, sample hold circuit is constructed by 2 op-amps and capacitor, but it is composed by 1 op-amp and capacitor on this circuit, so it is neglective total number of op-amps. This circuit needs initial reset cycle and reset cycles before starting every cyclic blocks. We call both initial reset and reset cycles no-conv cycle. The no-conv cycle wastes 1 clock cycle while S2 switch is ON state. The output of compara-

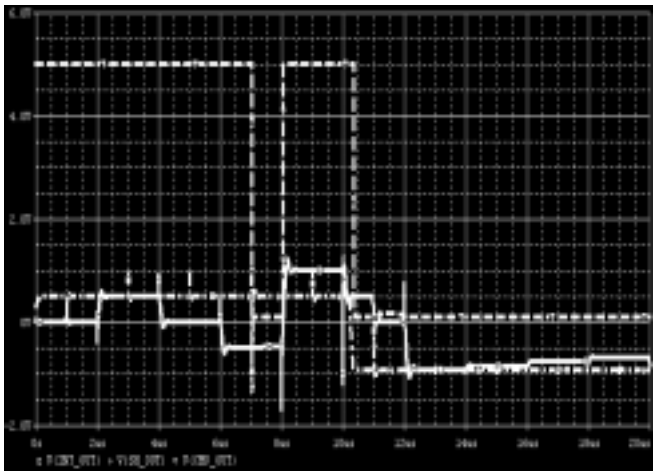

Figure 6: 2 blocks Cyclic sigma delta ADC: input=0.5V, sampling frequency=50kHz. Integrator output, Sample hold output and Comparator output.

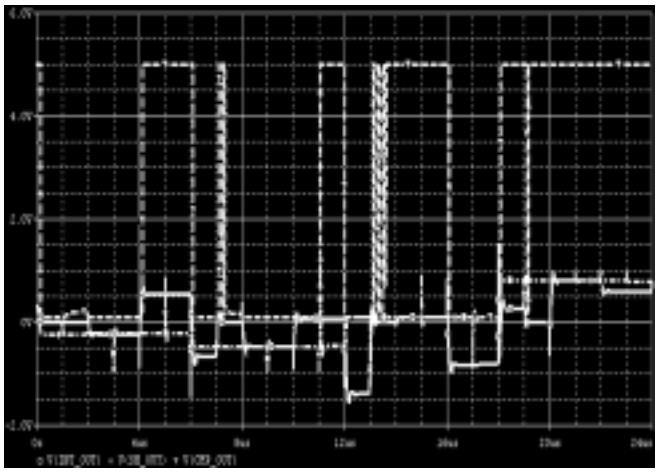

Figure 7: 4 blocks Cyclic sigma delta ADC: input=-0.23V, sampling frequency=50kHz. Integrator output, Sample hold output and Comparator output.

tor has the 3 functions that decides the sign bit of input voltage while initial reset and S3 switch are ON state, digital equivalent value while S3 switch is ON state without no-conv cycle and controls the reference voltage for feedback it to the integrator.

5. Simulation results

In this section, we verified the performance of new cyclic sigma delta ADC by Cadence Pspice A/D circuit simulator. It was confirmed that both 2 blocks cyclic and 4 blocks cyclic perform well on occasion of 8 clock cycles without no-conv cycles, sampling frequency which was 50kHz, reference voltage was $\pm 1.0V$, capacitor C1=20p(sample hold), capacitor C2=C3=0.2n(integrator) and capacitor C4=2n(inverse integrator voltage). One of the 2 blocks cyclic simulation results is shown in Figure.6. And also, one of the 4 blocks cyclic simulation result is shown in Figure.7. 34 simulations were performed by 2 blocks cyclic circuit. 66 simulations were performed by 4 blocks cyclic circuit. The miss code did not appear during both 2 blocks cyclic and 4 blocks cyclic simulations. The resolution of 2 blocks cyclic and 4 blocks is 4 bits and 6 bits, respectively. Both circuits did not work correctly when the capacitor value was changed, so we could not confirm robustness of capacitor matching.

6. Conclusions

In this paper, both 2 blocks cyclic and 4 blocks cyclic was verified by the circuit simulation, so it realized TDM cyclic sigma delta ADC. For realizing TDM cyclic sigma delta ADC, it is applied to new architecture of inverse integrator output circuit. Good simulation results were obtained, but it is restricted to low speed due to the simulator performance. Sigma delta ADC has the advantage of capacitor matching, but we could not verify it in this time. It proved SC circuit advantage of TDM. It can realize that perform AD conversion to the Voice band frequency, it needs to improve resolution much more. The resolution improvement of cyclic sigma delta ADC derives from increment of clock cycle and multiplexing cyclic block, but it degrades sampling rate, this demerit is avoided by parallel structure of a few cyclic sigma delta ADCs. Next challenge will be hardware implementation, verification of enhancing the clock cycle and the multiplexing, integration of the TDM system and the SDM system, reducing the clock phases for SC circuit, investigation of capacitor matching.

References

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