The Digital Charge Pump PLL

Pascal Acco†, Orla Feely‡ and Danièle Fournier-Prunaret†

†LESIA – Laboratoire d'Étude des Systèmes Informatiques et Automatiques, INSA, DGEI, 135 avenue de Rangueil, 31077 Toulouse, France.
e-mail: pascal.acco@insa-tlse.fr
and daniele.fournier@insa-tlse.fr

‡Department of Electronic and Electrical Engineering, University College Dublin
Belfield, Dublin 4, Ireland
e-mail: orla.feely@ucd.ie

Abstract

Modeling a digital phase-locked loop (PLL) is made difficult by the non-linear elements within the circuit, including quantization non-linearities. The application in which the system will be used often demands a high degree of flexibility in the design of non-linear Phase-Frequency Detectors (PFD) and non-linear filters. The mathematical analysis of such complex systems inevitably requires that approximations be made in modeling the non-linear components (such as the well-known case of the sinusoidal phase-detector). In this paper, the idea is to implement the simple principle of the charge-pump PLL (CP-PLL) in a digital circuit. Equations can be written for such a Digital CP-PLL (D-CP-PLL), and we can apply analysis techniques developed for the CP-PLL to this circuit. We obtain an exact mathematical equation with a more realistic model than the sinusoidal phase-detector. As we can run very fast and precise simulations of the system, the parameters can be found with a brute force optimisation technique. Using a full digital ring oscillator to implement the NCO we can implement the D-CP-PLL with basic digital building cells. As for the ring oscillators of the CP-PLL, this D-CP-PLL does not need any external clock as it uses its NCO signal and input signal to generate the input word of the NCO. Such a Digital PLL has no external clock and its parameters can be calculated automatically, moreover it can be digitally synthesised without any analog design.

1. Introduction

The CP-PPL is a mixed-signal circuit containing two analog parts: the filter and the voltage-controlled oscillator. We will present a fully digital version of this system. The two analog parts are replaced with a logic circuit which builds an approximation of the second-order PLL waveforms. The global structure is presented in fig. 1.

The different components are:

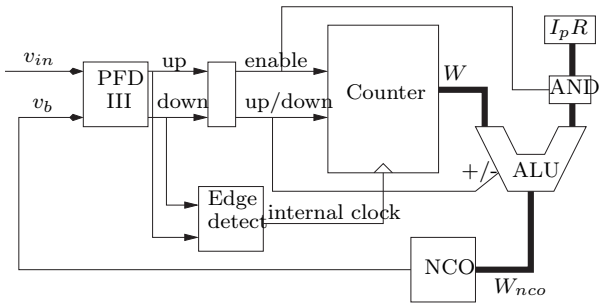

Figure 1: Digital CP-PLL proposed

The Phase Frequency Detector (PFD): its outputs control the counter and depends on the phase and frequency error between the feedback signal v_b and the input signal v_{in}. In this case, the PFD is a state machine whose diagram is shown in fig. 2. $+I_p$, 0 and $-I_p$ respectively correspond to the outputs UP and $\overline{DOWN}$, $\overline{UP}$ and $\overline{DOWN}$ and finally $\overline{UP}$ and $DOWN$.

The Counter and ALU: The counter counts up when the PFD state is $+I_p$, down when the state is $-I_p$ and does not count when it is 0. The counter can count internal reference clock edges or directly the NCO outputs edges or a multiple frequency of this output. These different possibilities will be discussed further. A constant value I_pR is added (resp. subtracted) to the counter word W when the PFD state is $+I_p$ (resp. $-I_p$). A null value is added when this state is 0 (the Enable signal is 0 and nulls the outputs of the AND gates).

The Numerically Controlled Oscillator (NCO): this oscillator generates a signal whose instantaneous frequency is an affine function of the input word given by the ALU. This output frequency is fed back via an N frequency divider or directly to

the PFD. This can be realised by a ring oscillator, as presented in [3]

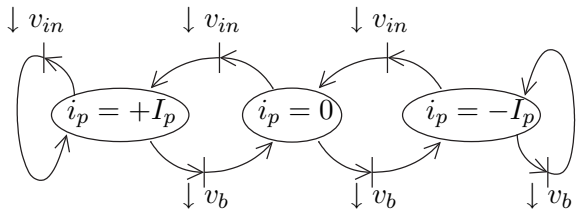

Figure 2: PFD state diagram (↓ means falling edge)

2. Backward and forward DCP-PLL

There are different ways to approximate the CP-PLL waveforms in a digital implementation. These solutions depend on the clock signal presented at the counter input. This signal can be generated from an external clock or directly from the NCO output. Good behaviour is obtained by generating a high frequency signal from the NCO. This high frequency signal is the XOR combination of all the inverter outputs of the NCO ring oscillator.

There exist no analytical models for any of these solutions because the NCO input changes between two changes of the PFD state machine. A simpler model is obtained by connecting the counter input to the PFD outputs: this has the advantage of presenting a constant word value at the NCO input between two changes of state of the PFD.

As for numerical integration, this leads to two approximations of CP-PLL waveforms: the backward and the forward waveforms, shown in fig. 3.

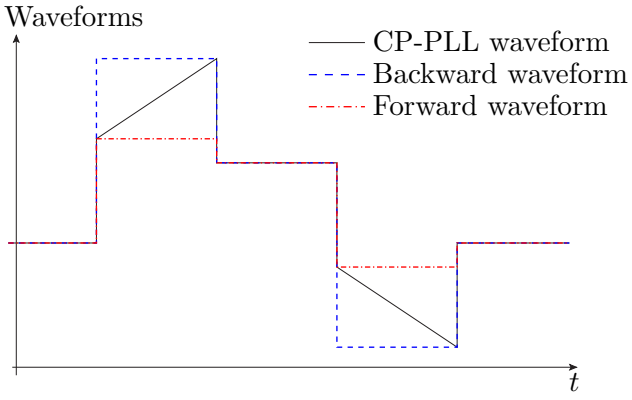

Figure 3: Forward and backward digitalisation of CP-PLL

The waveforms are obtained when the counter input is triggered at the rising edges of the UP and DOWN signals and the backward waveforms are obtained by using the falling edges of those signals.

3. DPLL non-linear model

A behavioural event-driven model has been written for the DCP-PLL using the same technique previously used for the CP-PLL [2]. This behavioural model can run fast and precise simulations and allows brute force optimisation, as for the CP-PLL [1]. An event-driven simulation is shown in fig. 4.

In this section we will present the nonlinear discrete model of the DCP-PLL. If we consider the D-PLL proposed we get an order-two set of non-autonomous nonlinear difference equations. The state variables chosen are shown in fig. 5, they are:

- w_k: The value of the word contained in the counter when the counting is not enabled between time t_k and t_{k+1}.

- τ_k: The time between the next falling edge of the feedback signal v_b and the time kT which corresponds to a falling edge of the input signal. When v_b is leading τ_k is negative, and when this signal is lagging τ_k is positive.

The expression for τ_{k+1} and w_{k+1} depends on the PFD state at times t_k and t_{k+1}. This leads to four different expressions depending on the PFD states, i.e., the sign of τ_k and τ_{k+1}. When τ_k (resp. τ_{k+1}) is positive the counter is counting up at time t_k (resp. t_{k+1}) and counting down when τ_k (resp. τ_{k+1}) is negative.

The expression for w_{k+1} can be unique if we use the following non-linear expression

$$w_{k+1} = w_k + sign(\tau_k) \tag{1}$$

We note that the equations of the forward DPLL are obtained by substituting terms I_pR by $I_pR - 1$ in the equations of the backward DPLL. We will therefore consider both DPLL equations using the generic term α instead of I_pR for the backward DPLL and I_pR-1 for the forward DPLL. The generic equation we will consider is then (2).

In the phase plane (w_k, τ_k) the model defines a point transformation $\mathcal{T}$ which maps the point X_k with coordinates (w_k, τ_k) to the point X_{k+1} with coordinates (w_{k+1}, τ_{k+1}). The four different expressions for τ_{k+1} divide the phase plane into four regions separated by two frontiers $\mathcal{F}_0$ and $\mathcal{F}_1$ shown in fig. 6. Those frontiers are respectively defined by the explicit equation (3) and two equations (4).

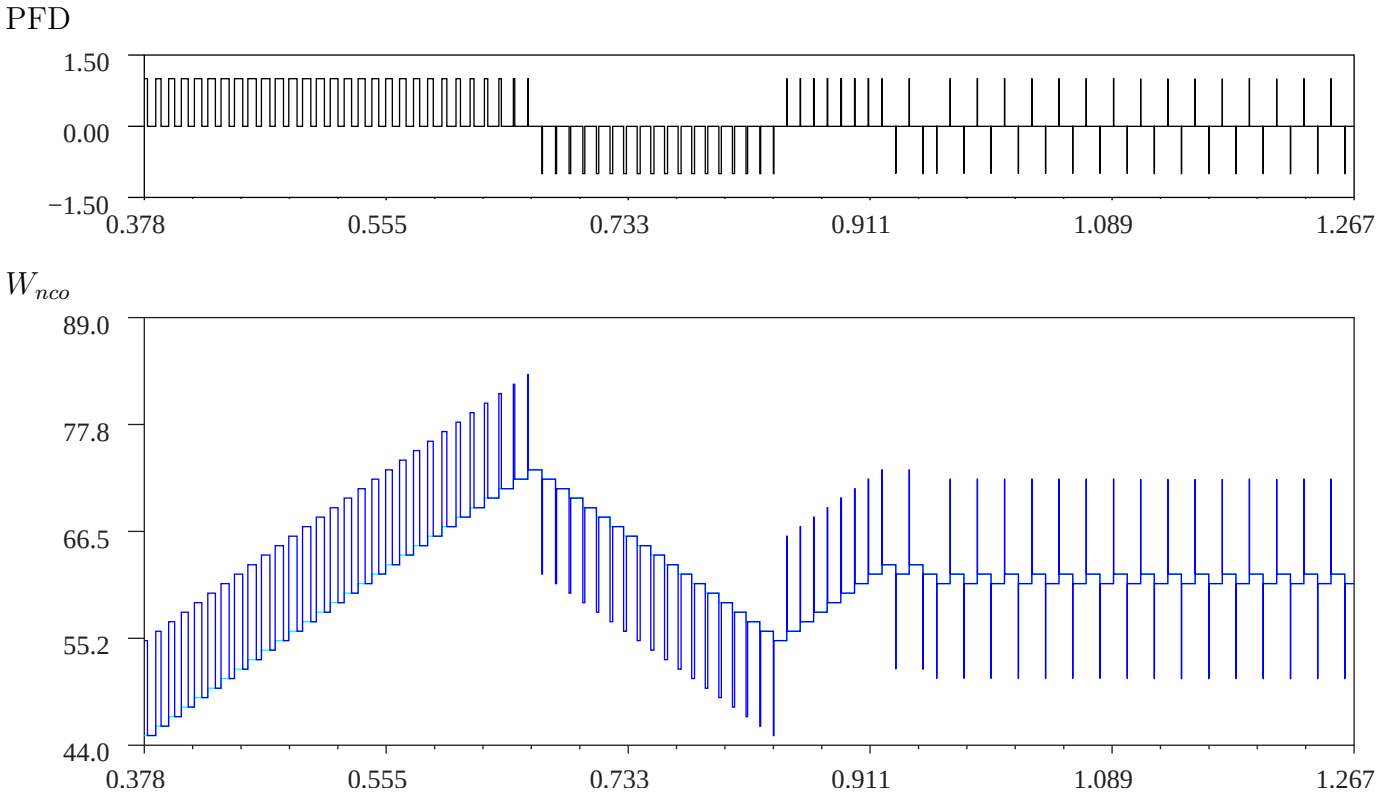

Figure 4: DCP-PLL simulation of the event driven model

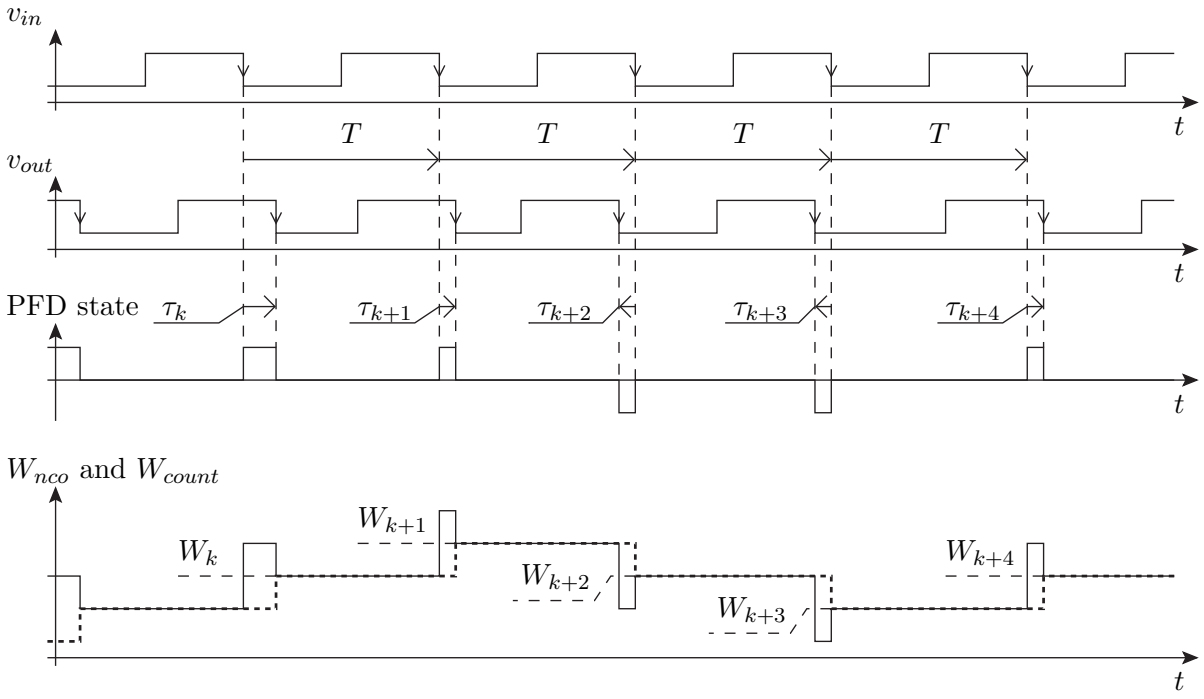

Figure 5: DPLL chronogram

$$\begin{cases} \begin{cases} w_{k+1} = w_k + 1 \\ \tau_{k+1} = \frac{1-(aW_k+b)(T-\tau_k)}{a(w_k+\alpha+1)+b} \end{cases} & \text{when } (w_k, \tau_k) \in \mathcal{R}_1 \\ \begin{cases} w_{k+1} = w_k - 1 \\ \tau_{k+1} = \frac{1-(aW_k+b)(T-\tau_k)-a\,\alpha\,\tau_k}{aw_k+b} \end{cases} & \text{when } (w_k, \tau_k) \in \mathcal{R}_2 \\ \begin{cases} w_{k+1} = w_k + 1 \\ \tau_{k+1} = \frac{1-(aW_k+b)(T-\tau_k)}{aw_k+b} \end{cases} & \text{when } (w_k, \tau_k) \in \mathcal{R}_3 \\ \begin{cases} w_{k+1} = w_k - 1 \\ \tau_{k+1} = \frac{1-(aW_k+b)(T-\tau_k)-a\,\alpha\,\tau_k}{a(w_k+\alpha+1)+b} \end{cases} & \text{when } (w_k, \tau_k) \in \mathcal{R}_4 \end{cases} \tag{2}$$

$$\mathcal{F}_0 : \tau_k = 0 \tag{3}$$

$$\mathcal{F}_1 : \tau_{k+1} = 0 \Longleftrightarrow \tag{4}$$

$$\begin{cases} 1-(a\,W_k+b)(T-\tau_k) = 0 & \text{when } \tau_k > 0 \\ 1-(a\,W_k+b)(T-\tau_k) - a\,\alpha\,\tau_k = 0 & \text{when } \tau_k < 0 \end{cases}$$

4. Conclusion

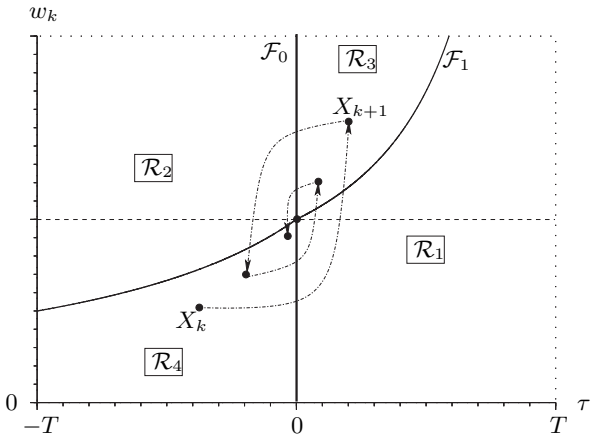

Figure 6: The four different regions

A digital version of the CP-PLL has been proposed in this paper. Its Phase Detector is made by a Finite State Machine which is commonly used because it allows a wide range of locking. A piece-wise non-linear model of this D-CP-PLL has been written. The brute force optimisation method used on the CP-PLL presented in [1] could then be used to design automatically the D-CP-PLL.

This work should be validated by a transistor level simulation. A Verilog model of the digital part has been done. But although the NCO proposed is made using standard digital cells, its behaviour depends on analog phenomena between those cells. A mixed simulation of this system should be performed in the future to validate the equations.

References

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