Improved Noise Reduction and Frequency Stability of VCO with External Feedback Loop

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Abstract:

The integated circuit VCO is combined with PI controller and F toV converter as the feedback part to be a colsed - loop VCO circuit (CLVCO). This colsed - loop circuit can achieved both wide bandwidth for good frequency stability of VCO as well as good noise rejection. The experimental results show that CLVCO is independent of power supply variation, and the performance of VCO is greatly improved. The controller design for optimum output response and minimizes the effected of VCO noise is also discussed.

1. Introduction

Voltage controlled oscillators (VCO's) are widely uesd in such application as phase - locked loops (PLL) , frequency synthesizers, FM modulators, clock recovery and many others. Most of the research works of VCO is the attempt to improve the temparature stability of the VCO's frequency at high frequencies [1] - [4]. The VCO phase noise in the PLL is not attenuated by the loop in the range of interest [5]. Thus it is usually necessary to resort to an off chip, high Q VCO. The other important performance of the VCO is the frequency stability and the VCO noise due to the voltage drift effected by the d.c. or a.c. noise coupling at the input of VCO.

This paper presents the closed-loop VCO (CLVCO) with a frequency - to - voltage (FVC) as the feedback element [6]. The PI - controller is designed for CLVCO by mean of the symmetrical optimum [7] in order to minimized the affect of d.c. and a.c. disturbances and to get the optimum output response. Thus we can use a low performance on - chip VCO, while the frequency stability and the VCO noise suppression are greatly improved. The experimental results confirm the validity of the proposed strategy.

2. Closed- Loop VCO Configuration

The proposed closed - loop VCO circuit is shown in Fig. 1. An ordinary VCO is configured in a feedback loop. The output of the VCO is first devided down to an intermediate frequency where a frequency - to - voltage converter (FVC) could be easily designed. The FVC then produces a voltage output that is proportional to the input frequency. This output is subtracted from a reference voltage and the error signal is subjected to the PI - controller which is designed for CLVCO by mean of the symmetrical optimum to minimizes the affect of d.c. and a.c. disturbances and to get the optimum output response.

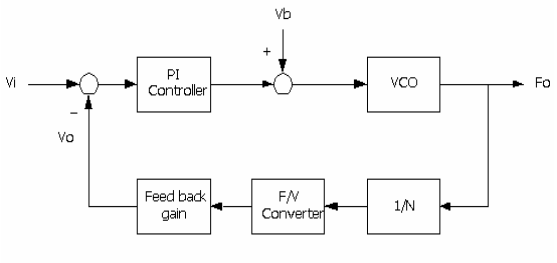


Fig.1 Closed - loop VCO configuration.

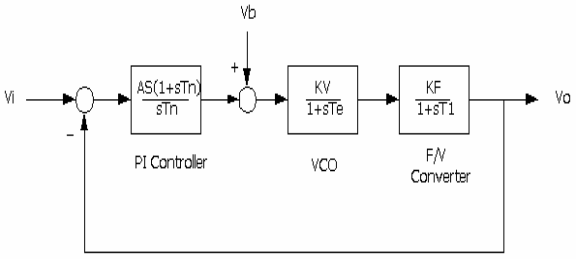


Fig. 2 Block diagram of the closed - loop VCO.

The controller F_R (s) has a pole at d.c. (integrator), then the steady state error signal will be zero and the output of the F/V will be equal to the input reference. The output frequency will thus be equal to

$$f_o = \frac{N}{K_F} V_i \qquad (1)$$

Where K_F is the gain of the FVC in V/H_z.

Fig. 2 shows the block diagram of the closed-loop VCO with the nature of the signal shown at each point. The FVC is modeled by first - order delay with it's gain K_F. From Fig. 2 we can find the open - loop transfer function as follow;

$$F_O(s) = \frac{A_R(1+sT_n)}{sT_n} \cdot \frac{K_V}{1+sT_e} \cdot \frac{K_F}{1+sT_1} \quad (2)$$

The PI - controller is in the form of proportional gain, phase advance term and the integral element ;
$A_R(1+sT_n)/sT_n$

Where A_R is the proportional gain.
T_n is the integral time constant.
T_e is the time delay of VCO.
T_1 is the time delay of FVC.
K_V is the gain constant of VCO,and
K_F is the gain constant of FVC.

If a system to be controlled includes $T_1 > 4\ T_e$, the controller for the system should be designed in accordance with the symmetrical optimum. Hence the optimization formula for the proportional gain and the integral time constant are as follow.

$$T_n = 4\ T_e K_2 \quad (3)$$

$$A_R = \frac{T_1}{2K_F K_V T_e} \cdot K_1 \quad (4)$$

Where $K_1 = 1 + \frac{T_e^2}{T_1^2}$ and $K_2 = \frac{K_1}{(1+\frac{T_e}{T_1})^3}$

3. Experimental Results

We implement the closed-loop VCO with respect to Fig. 1. The on-chip VCO is MC14046B having the maximum frequency output 1.9 MHz with V_{DD} = 15 volt. The feedback path composed of FVC used with integrate circuit of LM 331 and the frequency devider (1/N) is equal to 1/60 , and feedback gain is 4.5. The controller is designed for CLVCO according to the symmetrical optimum approach and based on the delay time of the VCO (Te = 20ms) and the delay time of FVC (T1 = 100ms).

3.1 Transient Response of CLVCO

The transient response measurement of CLVCO is setup with respect to Fig. 2. This measurement the output of FVC is the voltage signal (Vo) then it is convenient to be measured by digital storage oscilloscope as the output response of the CLVCO. The Vi is the input command and the Vb is the second input which used for measurement the output response due to d.c./a.c. signal or noise coupling at this input.

3.1.1 Output Response to Step Input

Fig.3 shows the output response of CLVCO to the step input command comparing with opened - loop response. According well - designed of controller shows a rapid response to change in input control voltage with fast rise time and no overshoot. The CLVCO has more wide bandwidth than the opened – loop VCO is, of course, it's ability to follow changes in Vi and reflect these changes accurately in the way that Fo changes.

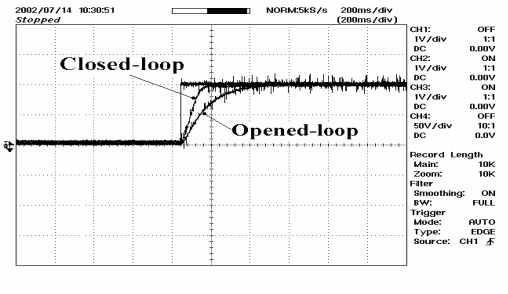


Fig. 3 Output response of CLVCO to the step input comparing with opened-loop response.

3.1.2 Output Response to Step D.C. Signal Coupling

Fig. 4 shows the output response of CLVCO to the step d.c. signal coupling (Vb) . The CLVCO has the ability to suppress the d.c. signal coupling.

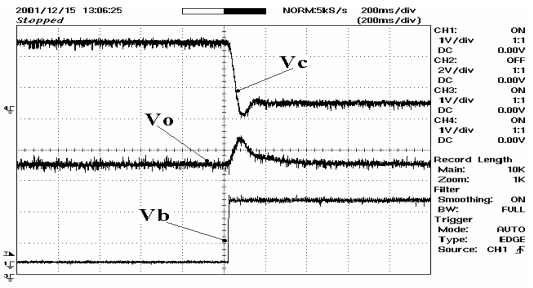


Fig. 4 Output response of CLVCO to the step d.c. signal coupling (Vb).

3.1.3 Output Response to Step A.C. Signal Coupling

Fig. 5 shows output response to step a.c. signal coupling (Vb) . The CLVCO also has the ability to suppress the a.c. signal coupling at the frequency more than 2 MHz.

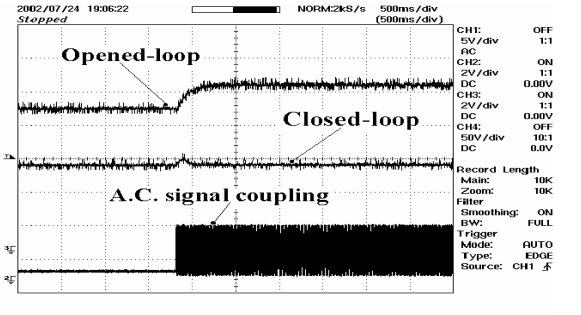
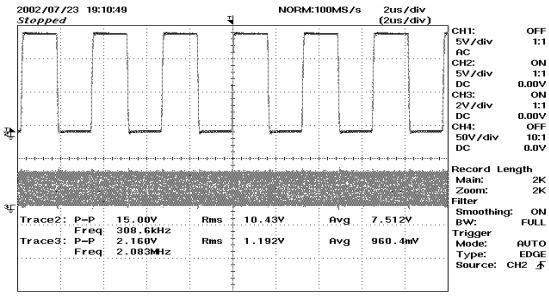
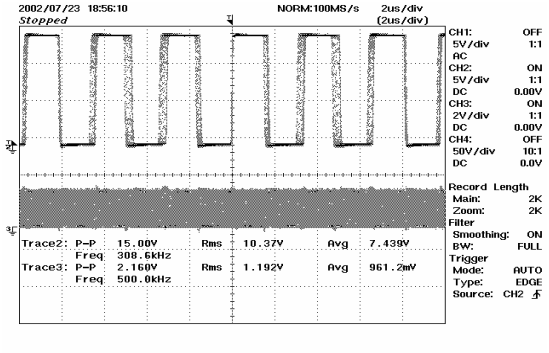


Fig. 5 Output response to step a.c. signal coupling (Vb).

Fig. 6 shows the ability of CLVCO to suppress the high frequency more than 2 MHz. of a.c. signal coupling.



(a) Vb = 2 MHz



(b) Vb = 500 KHz

Fig. 6 Output frequency (Fo) of VCO can suppress the high frequency a.c. signal coupling, (a) no phase jitter , (b) occuring phase jitter.

3.1.4 Output Response to Step Noise Coupling

Fig. 7 shows the output response of CLVCO to step noise coupling (Vb). The CLVCO also has the ability to suppress the VCO noise coupling.

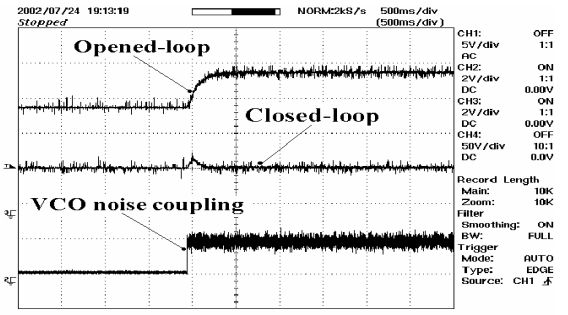
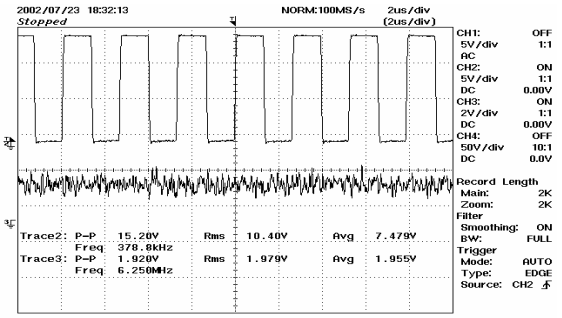
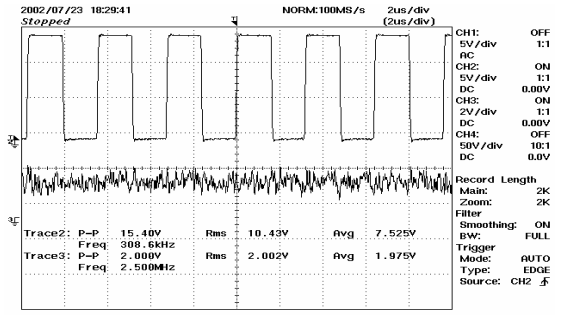


Fig. 7 Output response to step noise coupling (Vb).

The ability of CLVCO to suppress the VCO noise coupling is shown in Fig. 8.



(a) Opened - loop VCO



(b) Closed - loop VCO

Fig. 8 Output frequency (Fo) of VCO when injected the VCO noise, (a) opened - loop VCO , (b) closed - loop VCO.

3.2 Frequency Stability of CLVCO

The frequency stability of CLVCO measurement can be conducted by measuring the output frequency (Fo) of VCO which affected by the variation of the amplitude and frequency of the d.c. / a.c. signal and the VCO noise coupling and the variation of d.c. power supply. The

measured datas can be ploted as the graphs shown in Fig. 9, Fig. 10, Fig. 11 and Fig. 12 respectively.

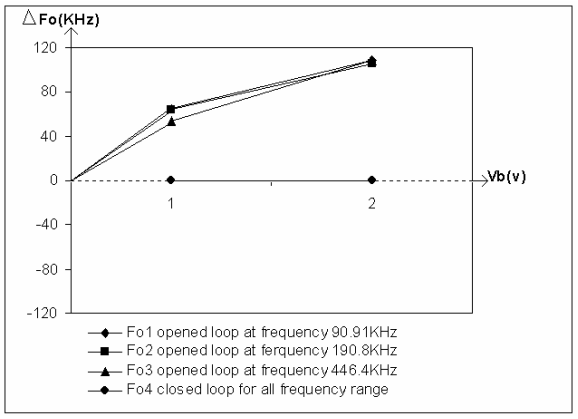


Fig. 9 Frequency deviation due to d.c. signal coupling.

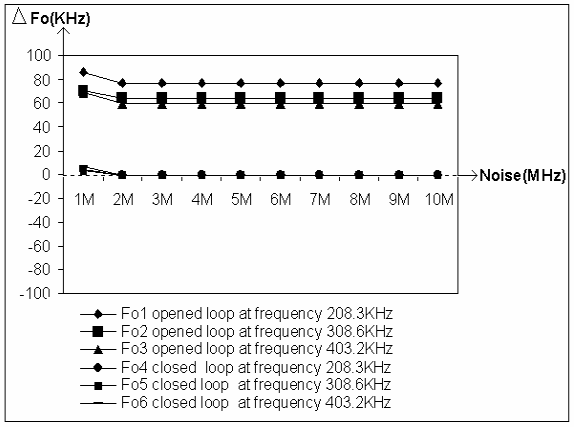


Fig.10 Frequency deviation due to high frequency a.c. signal coupling.

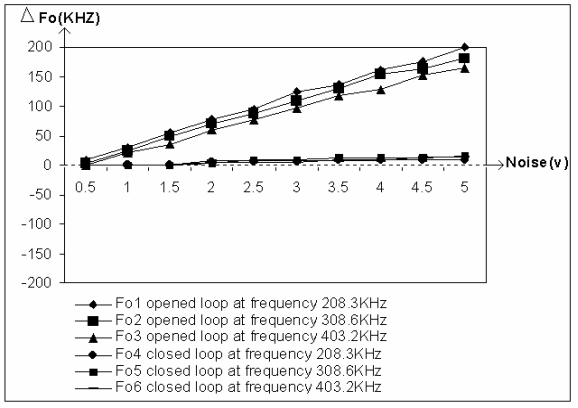


Fig.11 Frequency deviation due to VCO noise coupling.

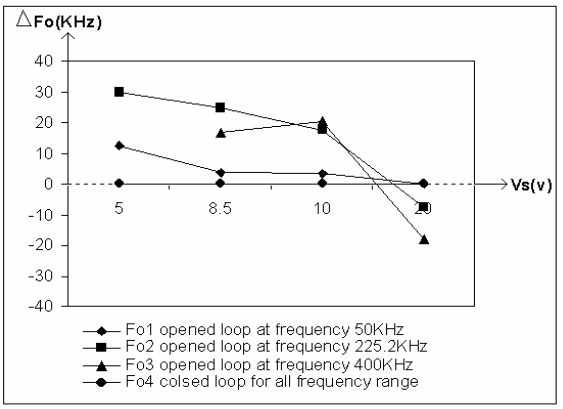


Fig.12 Frequency deviation due to d.c. power supply variation.

4. Conclusion

The on - chip VCO with external feedback loop shows that well design of controller achieves both a large bandwidth for good frequency stability of VCO as well as good noise rejection. The measured experimental results from the CLVCO shown a fast output response is the performance of wide operation bandwidth, good frequency stability, effectively noise suppression and insensitivity to power supply variations.

References

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