

## 電子情報通信学会DC研究会主催 特別講演会

### Advanced Embedded Memory Testing

このたび、DC研究会ではオランダ デルフト工科大学のSaid Hamdioui氏を迎えて、LSIメモリテストに関する講演会を開催することになりました。近年SoCにおけるメモリ占有率は増加する一方であり、メモリテスト手法はテストコストおよび品質を大きく左右する要因の一つとなっています。本講演では、シングルポートおよびマルチポートSRAMにおいて現れる故障を取り上げ、各故障モデルに適したテストアルゴリズムについて解説します。メモリテストやDFTの専門家だけでなく、LSI設計者や製造部門関係者、また大学関係者の方々も対象としていますので、多くの方々のご参加をお待ちしています。

日時	2008年11月20日(木) 10:00~17:00
会場	機械振興会館 6D-1会議室 〒105-0011 東京都港区芝公園3-5-8 <a href="http://www.ieice.org/jpn/about/syozai.html">http://www.ieice.org/jpn/about/syozai.html</a>
題目	Advanced Embedded Memory Testing 講師 Said Hamdioui氏 (オランダ デルフト工科大学)
概要	講師の紹介および講演内容詳細については、次ページ以降をご参照ください。
定員	40名 (参加申込順)
申込締切	2008年11月18日(火)
参加費	無料
申込方法	E-mailにてタイトルを”メモリテスト講演会参加登録”として、氏名、所属を記載の上、下記申込先までお申し込みください。
申込・ 問合せ先	(株)ルネサステクノロジ 中尾 教伸, 山崎 枢 E-mail: {nakao.michinobu, yamasaki.kaname}@renesas.com
主催	(社)電子情報通信学会 DC研究会

# Tutorial description and outline

**Title: Advanced Embedded Memory Testing**

**Instructor:**

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## **Description:**

The cost of memory testing increases with every generation of new memory chips. New technologies are introducing new defect mechanisms that were unknown in the past. Precise fault modeling to design efficient tests is therefore essential in order to keep the test cost and test time within economically acceptable limits, while keeping a high product quality.

The objective of the course is to provide test engineers, memory and ASIC designers, researchers and managers with an overview of fault modeling and test design for memory devices. Traditional fault modeling and recent development in fault models for current and future technologies are covered, and well as their frequency of occurrence. Systematic methods are presented for designing and optimizing test patterns supported by industrial results. Future challenges in fault modeling and test design are highlighted.

Upon the completion of the course, the attendee will (a) have a good knowledge of practices in memory testing, (b) understand the major types of memory faults, (c) know which tests should be performed to target each fault class, (d) have a feeling of the effectiveness of each test, (e) have the capability to develop new tests for any observed new faulty behavior and optimize them for specific application, (f) choose appropriate test strategy to achieve a high fault coverage with the minimum cost, and (g) get insight into the direction and future of memory testing. These will help the engineers strike the right trade off between design effort, product quality, test cost and time-to market.

## **About Instructor:**

Dr. Said Hamdioui received the MSEE and PhD degrees (both with honors) from the Delft University of Technology, Delft, The Netherlands. He is currently a faculty member at Computer Engineering Lab of Delft University of Technology. Prior to joining Delft University, Hamdioui worked for Microprocessor Products Group at Intel Corporation (in Santa Clara and Folsom, California), for IP and Yield Group at Philips Semiconductors R&D (Crolles, France) and for DSP design group at Philips/ NXP Semiconductors (Nijmegen, The Netherlands). Hamdioui is the recipient of European Design Automation Association (EDAA) Outstanding Dissertation Award 2001, due to invented memory test techniques that have a wide-spread proliferation in the chip design industry. His research interests include VLSI Design & Test (memory test, fault tolerance, reliability, etc.) and Nanotechnology (Nandevices, defect tolerance, nano-architectures, reliability, etc).

Hamdioui published one book and over 50 conference and journal papers; many of them are results of the co-operation with different industrial partners. He consulted many companies (Intel, ST, Altera, Atmel, Infineon, ...) in the area embedded memory testing to improve their test coverage and enhance the outgoing product quality. He was the general co-chair of IEEE International Conference on Design and Technology of Integrated Systems in nanoscale Era DTIS07. He is a member of the program committees of different international conferences (IEEE European Test Symposium ETS, IEEE International Conference on Computer Design ICCD, IEEE International Design and Test Workshop IDT, DTIS, etc). He is a reviewer for major journals and conferences: IEEE Trans. CAD, IEEE Trans. on VLSI, IEEE Trans. on Computers, IEEE Design & Test of Computers, Intl. Test Conf., IEEE VLSI Test Symposium, European Test Symposium and several others. Hamdioui is a senior member of the IEEE.

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  - b. Trends in SoC design and test
  - c. Trends in failure mechanisms
  - d. Test philosophy
  - e. Manufacturing test flow
  - f. Test trade-offs
- 2. Traditional faults models and tests**
  - a. Models/levels of abstraction
  - b. Reduced memory model
  - c. Memory cell array faults
  - d. Address decoder faults
  - e. Peripheral circuit faults
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  - g. Industrial results
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  - b. Static versus dynamic faults
  - c. Simple versus linked faults
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  - c. Dynamic memory cell array faults (dMCAFs)
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  - b. Test approach classification
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- 7. Future challenges in trends in fault modeling and tests**
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  - b. Memory faults
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