

IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences
Special Section on “Design Methodologies for System on a Chip”
 (July 2019 Issue)

The IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences announces a forthcoming Special Section on Design Methodologies for System on a Chip to be published in July 2019.

The objective of the special section is to discuss new theoretical or practical developments and techniques in Design Methodologies for System on a Chip. The special section solicits paper submission from anyone in this field, and especially from people who present papers in the 31st Workshop on Circuits and Systems. The authors working in this area are strongly encouraged to submit original research papers on the topics which include the following areas:

Design environments and tools	Embedded system	Reconfigurable system
Multi/Many core design	Network-on-a-Chip design	System level design
IP-based design	High-level synthesis	Logic synthesis/verification
Layout design/verification	3D-IC	Analog CAD
Timing analysis	Testing/Diagnosis	Low power design
Reliable design	Secure design	Noise-aware design
Design for Manufacturability	Lithography CAD	

Notes to the Authors:

All manuscripts should be prepared according to the guideline given in “Information for Authors” which is available at http://www.ieice.org/eng/shiori/mokuji_ess.html. At least one of the authors must be an IEICE member when the manuscript is submitted for review. It is recommended that the lengths of a paper and a letter for this special section are within 8 and 2 printed pages, respectively.

This special section will accept papers only by electronic submission. Prospective authors are requested to follow carefully the submission process described below.

1. Submit a complete paper and **electronic files (Word/TeX files, figures, authors’ photos and biography)** for publishing using the IEICE Web site, https://review.ieice.org/regist/regist_baseinfo_e.aspx. Authors should choose the “[Special-SO] Design Methodologies for System on a Chip” as a “Journal/Section”. Do not choose “[Regular-EA]”. See details at http://www.ieice.org/eng/shiori/mokuji_ess.html.
2. Agree to the “Copyright Transfer and Page Charge Agreement” via the same website as paper submission.

The manuscript will undergo the standard review process of the IEICE Transactions on Fundamentals.

Deadline of Submission: September 7, 2018

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Please note that if the manuscript is accepted for publication, all authors should pay the page charges covering partial cost of publication around March, 2019. If payment is not completed by 15 April, 2019, your manuscript will be handled as rejection.