The IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences announces a forthcoming Special Section on Design Methodologies for System on a Chip to be published in July 2017.

The objective of the special section is to discuss new theoretical or practical developments and techniques in Design Methodologies for System on a Chip. The special section solicits paper submission from anyone in this field, and especially from people who present papers in the 29th Workshop on Circuits and Systems. The authors working in this area are strongly encouraged to submit original research papers on the topics which include the following areas:

- Normally-off computing
- Reconfigurable system
- System level design
- Logic synthesis/verification
- Analog CAD
- Low power design
- Noise-aware design
- Design environments and tools
- Multi/Many core design
- IP-based design
- Layout design/verification
- Timing analysis
- Reliable design
- Design for Manufacturability
- Network-on-a-Chip design
- High-level synthesis
- 3D-IC
- Testing/Diagnosis
- Secure design
- Lithography CAD

**Notes to the Authors:**

All manuscripts should be prepared according to the guideline given in “Information for Authors” which is available at http://www.ieice.org/eng/shiori/mokuji_ess.html. At least one of the authors must be an IEICE member when the manuscript is submitted for review. It is recommended that the lengths of a paper and a letter for this special section are within 8 and 2 printed pages, respectively.

This special section will accept papers only by electronic submission. Prospective authors are requested to follow carefully the submission process described below.


2. Agree to the “Copyright Transfer and Page Charge Agreement” via the same website as paper submission.

The manuscript will undergo the standard review process of the IEICE Transactions on Fundamentals.

**Deadline of Submission:**

September 9, 2016  
September 14, 2016 (Extended!)

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