The IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences announces a forthcoming Special Section on VLSI Design and CAD Algorithms to be published in December 2016. The objective of the special section is to discuss new theoretical or practical developments and techniques in VLSI design and CAD algorithms. The special section solicits paper submission from anyone in this field, and especially from people who present papers at ASP-DAC 2016. The authors working in this area are strongly encouraged to submit original research papers on the topics which include, but are not limited to, the following areas:

- VLSI design methodology
- VLSI architecture
- Logic synthesis
- Low power design
- Simulation (device, process, circuit, logic, high-level, etc.)
- Test pattern generation
- Co-design
- Formal verification
- High-level synthesis
- Layout verification
- Floor-planning and placement
- Routing
- Analog circuit design
- Cell/module design
- System level design
- Design for testability

**Notes for Authors:**

All manuscripts should be prepared according to the “Information for Authors” which is available in http://www.ieice.org/eng/shiori/mokuji_ess.html. It is recommended that the lengths of a paper and a letter for this special section are within 8 and 2 printed pages, respectively. For the submission, at least one author of each paper must be a member of the IEICE.

This special section will accept papers only by electronic submission. Prospective authors are requested to follow carefully the submission process described below.


The manuscript will undergo the standard review process of the IEICE Transactions on Fundamentals.

*Authors must agree to the "Copyright Transfer and Page Charge Agreement" via electronic submission.

**Deadline of Submission:**

March 10, 2016

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